ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a plurality of bit line pairs, each of which includes a first bit line and a second bit line, a plurality of memory cells which are coupled to said first bit line, and store electric charge in capacitors, a dummy cell which is coupled to a second bit line, and is charged with a predetermined potential, a sense amplifier which amplifies a potential difference between the first bit line and the second bit line, and a control circuit which charges said dummy cell with the predetermined potential only for a fixed time period.